CLAIMS

We claim:

1. A pad structure for providing electrical contact for interconnections in a semiconductor wafer comprising:

a metal layer; and

a dielectric layer having:

a plurality of vias,

wherein the metal layer fills the vias to form plugs, and

a plurality of dummy structures disposed within the pad structure,

wherein the dummy structures are inactive areas configured to increase the planarity of the metal layer.

2. The pad structure of claim 1, further comprising a barrier layer disposed between the dielectric layer and the metal layer.

3. The pad structure of claim 1, further comprising a seed layer disposed between the dielectric layer and the metal layer.

4. The pad structure of claim 1, further comprising a cover layer disposed on the surface of the metal layer and dielectric layer.

5. The pad structure of claim 1, wherein the metal layer is copper.

6. The pad structure of claim 1, wherein the plurality of dummy structures includes the same material as the dielectric layer.

7. The pad structure of claim 1, wherein the plurality of dummy structures includes a metal.

8. The pad structure of claim 1, wherein the dielectric layer is formed with a recessed area and a non-recessed area, wherein the plurality of dummy structures are disposed within the recessed area, wherein the metal layer is deposited to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, and wherein the metal layer is electropolished to expose the non-recessed area.

9. The pad structure of claim 8, wherein the recessed area has a depth corresponding to a thickness of the metal layer to remain within the recessed area after electropolishing and an offset height corresponding to a distance between a surface of the non-recessed area to be exposed after electropolishing and a surface of the metal layer to remain within the recessed area after electropolishing.

10. The pad structure of claim 9, wherein the exposed non-recessed area is removed to a depth equal to the offset height.

11. A structure formed on a semiconductor wafer comprising:

a dielectric layer formed on the semiconductor wafer having a recessed area and a non-recessed area;

a plurality of dummy structures formed within the recessed area,

wherein the dummy structures are inactive areas configured to increase the planarity of a metal layer subsequently formed on the dielectric layer;

a metal layer formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, wherein the metal layer is electropolished to expose the non-recessed area.

12. The structure of claim 11, wherein the recessed area has a depth corresponding to a thickness of the metal layer to remain within the recessed area after electropolishing and an offset height corresponding to a distance between a surface of the non-recessed area to be exposed after electropolishing and a surface of the metal layer to remain within the recessed area after electropolishing.

13. The structure of claim 12, further comprising removing the exposed non-recessed area to a depth equal to the offset height.

14. The structure of claim 13, wherein the offset height is between about 5 nanometers to about 100 nanometers.

15. The structure of claim 11, wherein the metal layer is formed by depositing the metal layer.

16. The structure of claim 11, wherein the metal layer is formed by electroplating the metal layer.

17. The structure of claim 11,

wherein each dummy structure in the plurality has a width,

wherein the metal layer has a thickness,

wherein the thickness is based on the metal layer formed on the non-recessed area, and

wherein a ratio of the width to the thickness is between about 0.1 to about 1.

18. The structure of claim 17, wherein the ratio is 0.3.

19. The structure of claim 11,

wherein dummy structures in the plurality are spaced apart from each other by a distance,

wherein the metal layer has a thickness,

wherein the thickness is based on the metal layer formed on the non-recessed area, and

wherein a ratio of the distance to the thickness is between about 1 to about 5.

20. The stucture of claim 19, wherein the ratio is less than 2.

21. The structure of claim 11, further comprising:

a barrier layer formed on the dielectric layer before forming the metal layer.

22. The structure of claim 11, further comprising:

a seed layer formed on the dielectric layer before forming the metal layer.

23. The structure of claim 11, further comprising:

a cover layer formed on the semiconductor wafer after electropolishing the metal layer.

24. The structure of claim 11, wherein the recessed area is a wide trench configured to form an interconnection when filled with the metal layer.

25. The structure of claim 11, wherein the recessed area is a large rectangular structure configured to form a pad when filled with the metal layer.

26. The structure of claim 25, wherein the exposed non-recessed area is removed beyond a surface of the electropolished metal layer to form a pad that protrudes beyond the dielectric layer to facilitate contact between the pad and a probe used for electrical testing.

27. The structure of claim 25, wherein the large rectangular structure has rounded corners.

28. The structure of claim 11, wherein the metal layer is copper.

29. The structure of claim 11, wherein the plurality of dummy structures includes the same material as the dielectric layer.

30. The structure of claim 11, wherein the plurality of dummy structures includes a metal.

31. A structure formed on a semiconductor wafer comprising:

a dielectric layer formed on the semiconductor wafer,

wherein the dielectric layer is formed with a recessed area and a non-recessed area;

a plurality of dummy structures formed within the recessed area;

a barrier layer formed to cover the recessed area, the non-recessed area, and the plurality of dummy structures; and

a metal layer formed to fill the recessed area and cover the non-recessed area and the plurality of dummy structures, wherein the metal layer is electropolished to expose the barrier layer deposited on the non-recessed area, and wherein the exposed barrier layer is removed at a first rate and the non-recessed area of the dielectric layer is removed at a second rate.

32. The structure of claim 31, wherein the exposed barrier layer and the non-recessed area of the dielectric layer have even surfaces after the exposed barrier layer is removed at a first rate and the non-recessed area of the dielectric layer is removed at a second rate.

33. The structure of claim 31, wherein the exposed barrier layer protrudes beyond the non-recessed area after the exposed barrier layer is removed at a first rate and the non-recessed area is removed at a second rate.

34. The structure of claim 31, wherein the first rate is equal to the second rate.

35. The structure of claim 31, wherein the first rate is lower than the second rate.

36. The structure of claim 31, wherein the exposed barrier layer is removed at a third rate and wherein the non-recessed area of the dielectric is removed at a fourth rate.

37. The structure of claim 36, wherein the third rate is higher than the fourth rate.

38. The structure of claim 37, wherein the fourth rate is zero.

39. The structure of claim 36, wherein the fourth rate is higher than the third rate.

40. The structure of claim 39, wherein the third rate is zero.

41. The structure of claim 36, wherein the first rate is higher than the second rate.

42. The structure of claim 36, wherein the exposed barrier layer and the non-recessed area have even surfaces after the exposed barrier layer is removed at a third rate and the non-recessed area is removed at a fourth rate.

43. The structure of claim 36, wherein the exposed barrier layer protrudes beyond the non-recessed area after the exposed barrier layer is removed at a third rate and the non-recessed area is removed at a fourth rate.